Electronic Version
Stylesheet Version v1.1.1

Claims

[c1] What is claimed is:

1.A high-to-low level shifter being coupled to a first voltage and a second voltage, wherein the first voltage is larger than the second voltage, the high-to-low level shifter comprising:

an inverter for receiving an input signal and generating an inverse input signal, wherein the inverter operates at the first voltage; and

a level shifter for generating an output signal according to the input signal and the inverse input signal, wherein the level shifter operates at the second voltage, the logic level of the output signal corresponds to the second voltage, and the logic value of the output signal corresponds to the input signal.

[c2] 2.The high-to-low level shifter of claim 1, wherein the level shifter comprises a pull-up unit and a pull-down unit.

[c3] 3.The high-to-low level shifter of claim 2, wherein the pull-up unit is for receiving the input signal, the pull-down unit is for receiving the inverse input signal, and the pull-up unit and the pull-down unit are coupled to

the output signal.

[c4] 4.The high-to-low level shifter of claim 2, wherein the pull-up unit is for receiving the inverse input signal, the pull-down unit is for receiving the input signal, and the pull-up unit and the pull-down unit are coupled to the output signal.

[c5] 5.The high-to-low level shifter of claim 2, wherein the pull-up unit is an NMOS transistor.

[c6] 6.The high-to-low level shifter of claim 2, wherein the pull-down unit is an NMOS transistor.

[c7] 7.The high-to-low level shifter of claim 2, wherein both the pull-up unit and the pull-down unit are high voltage devices.

[c8] 8.The high-to-low level shifter of claim 1, wherein the level shifter is set inside an integrated circuit.

[c9] 9.The high-to-low level shifter of claim 1, wherein the inverter is set outside an integrated circuit.

[c10] 10.A high-to-low level shifter comprising:
a first transistor for receiving a first input signal; and
a second transistor for receiving a second input signal which is the inverse of the first input signal, wherein the first transistor and the second transistor are coupled to

an output end for outputting an output signal, the logic value of the output signal corresponds to the first input signal and the second input signal;
wherein the logic level of the first input signal and the second input signal correspond to a first voltage, the logic level of the output signal corresponds to a second voltage, and the first voltage is larger than the second voltage.

[c11] 11.The high-to-low level shifter of claim 10, wherein both the first transistor and the second transistor are NMOS transistors.

[c12] 12.The high-to-low level shifter of claim 10, wherein the first transistor and the second transistor operate at the second voltage.

[c13] 13.The high-to-low level shifter of claim 10, wherein the first transistor is coupled to the second voltage.

[c14] 14.The high-to-low level shifter of claim 10, wherein the high-to-low level shifter is set inside an integrated circuit.

[c15] 15.The high-to-low level shifter of claim 10, wherein the first voltage is 3.3V.

[c16] 16.The high-to-low level shifter of claim 10, wherein the

second voltage is less than 0.9V.